UNIT-3 MPHYCC-7

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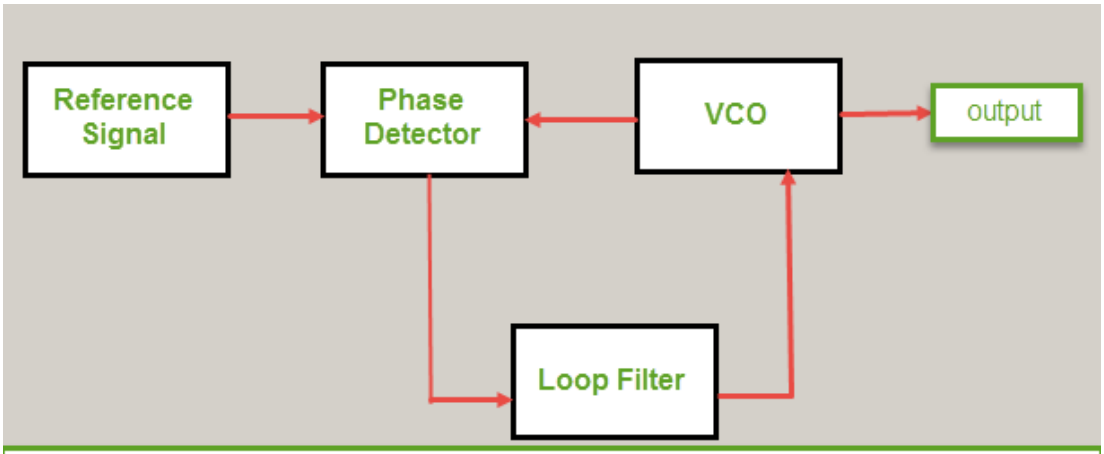
Phase Locked Loop

Phase locked loop basics

A phase locked loop, PLL, is basically of form of servo loop. Although a PLL performs its actions on a radio frequency signal, all the basic criteria for loop stability and other parameters are the same. In this way the same theory can be applied to a phase locked loop as is applied to servo loops.



BASIC DIAGRAM OF PHASE LOCKED LOOP

A basic phase locked loop, PLL, consists of three basic elements:

Phase comparator / detector: As the name implies, this circuit block within the PLL compares the phase of two signals and generates a voltage according to the phase difference between the two signals. This circuit can take a variety of forms.

Phase locked loop operation

The basic concept of the operation of the PLL is relatively simple, although the mathematical analysis and many elements of its operation are quite complicated

The diagram for a basic phase locked loop shows the three main element of the PLL: phase detector, voltage controlled oscillator and the loop filter.

In the basic PLL, reference signal and the signal from the voltage controlled oscillator are connected to the two input ports of the phase detector. The output from the phase detector is passed to the loop filter and then filtered signal is applied to the voltage controlled oscillator.

The Voltage Controlled Oscillator, VCO, within the PLL produces a signal which enters the phase detector. Here the phase of the signals from the VCO and the incoming reference signal are compared and a resulting difference or error voltage is produced. This corresponds to the phase difference between the two signals.

The error signal from the phase detector passes through a low pass filter which governs many of the properties of the loop and removes any high frequency elements on the signal. Once through the filter the error signal is applied to the control terminal of the VCO as its tuning voltage. The sense of any change in this voltage is such that it tries to reduce the phase difference and hence the frequency between the two signals. Initially the loop will be out of lock, and the error voltage will pull the frequency of the VCO towards that of the reference, until it cannot reduce the error any further and the loop is locked.

When the PLL, phase locked loop, is in lock a steady state error voltage is produced. By using an amplifier between the phase detector and the VCO, the actual error between the signals can be reduced to very small levels. However some voltage must always be present at the control terminal of the VCO as this is what puts onto the correct frequency.

The fact that a steady error voltage is present means that the phase difference between the reference signal and the VCO is not changing. As the phase between

these two signals is not changing means that the two signals are on exactly the same frequency.

The phase locked loop, PLL is a very useful building block, particularly for radio frequency applications. The PLL forms the basis of a number of RF systems including the indirect frequency synthesizer, a form of FM demodulator and it enables the recovery of a stable continuous carrier from a pulse waveform. In this way, the phase locked loop, PLL is an essential RF building tool.