MPHYEC-1F Measurement and Instrumentation 2020

Unit 3 Notes (3)

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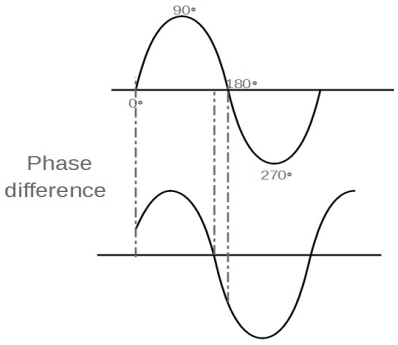
Phase Locked Loop

A Phase Locked Loop (PLL) is a feedback-based circuit which produces a signal that replicates its input signal (which usually is a sinusoidal signal of a variable freqency) in frequency by locking in to and continuously adjusting its phase difference with the input signal. The Phase Locked Loop circuit consists of three parts. They are, (1) Phase sensitive detector, (2) Low Pass Filter, and (3) Voltage controlled Oscillator. The output signal is generated by a Voltage controlled Oscillator (VCO). The purpose of the feedback loop is to always maintain the VCO output at same frequency as the frequency of the input signal by monitoring the phase difference between the input signal and the signal generated by the VCO and modifying the VCO output frequency according to this phase difference.

Basic Operation: The key to the operation of a PLL is the phase difference between two signals, the input and the generated signal and the ability to detect it. The information about the phase difference between these two signals is then used to control the frequency of the generated signal.

Phase Difference: Any sinusoidal waveform (in one dimension) can be represented using the equation $y = a \sin(\omega t - kx + \phi)$. Here, y is the displacement at a particular time and location, a represents the amlitude of the sinusoidal wave, ω is called the angular frequency which is 2π times the oscillation frequency, k is called the wave number, x represents the position where the displacement at time t is y. The quantity ϕ is called phase constant. If two identical waves represented by $y_1 = a \sin(\omega t - kx)$ and $y_2 = a \sin(\omega t - kx + \phi)$ are travelling in same direction, but with peaks at different positions at a given time, then their phase difference is represented by ϕ.



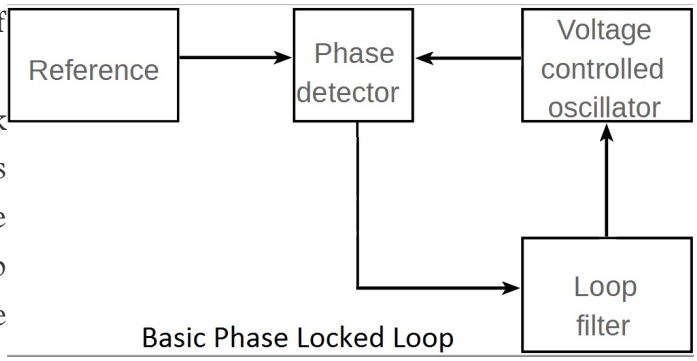
When two signals have different frequencies it is found that the phase difference between the two signals is always varying. The reason for this is that the time for each cycle is different and accordingly their phases are changing at different rates.

Thus, when two signals have exactly the same frequency, the phase difference between them is constant. When there is a phase difference between the two signals, it means that they do not reach the same point on the waveform at the same time. If the phase difference is fixed it means that one is lagging behind or leading the other signal by the same amount, i.e. they are on the same frequency.

Phase Lock Loop: A phase locked loop basically consists of a feedback loop or a servo loop. Thus the

same theory can be applied to a phase locked loop as is applied to feedback loops, except that in the feedback loops we have so far encountered were, the feedback quantity was the displacement, while in a PLL, the feedback quantity is phase difference.

A basic phase locked loop, PLL, consists of three basic elements:



Basic Phase Locked Loop

Phase comparator / detector: This circuit block within the PLL compares the phase of two signals and generates a voltage according to the phase difference between the two signals. Here, the two signals are the input or reference signal, and the VCO output signal.

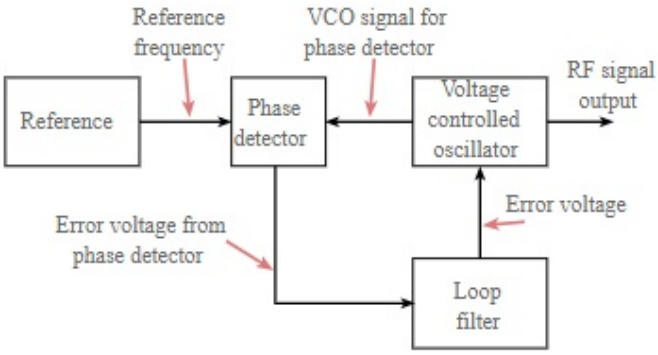
Voltage controlled oscillator (VCO): The voltage controlled oscillator is that part of the circuit that generates the output signal. Its frequency can be controlled over the operational frequency band of the feedback loop with help of a dc input voltage signal (which is provided by the phase comparator through the loop filter.

Loop filter: This is a Low pass filter that is used to filter the output from the phase comparator in the phase locked loop. It smooths out the phase comparator output, by removing the ac component from it. It can also be considered as an integrator that outputs a DC voltage that is the average of the phase comparator output over one cycle.

Phase Locked Loop Operation:

The basic concept of the operation of the PLL is relatively simple, although the mathematical analysis and many elements of its operation are quite complicated. The diagram for a basic phase locked loop shows the three main element of the PLL: phase detector, voltage controlled oscillator and the low pass loop filter.

In the basic PLL, reference signal and the signal from the voltage controlled oscillator are given to the two input ports of the phase detector. The phase detector outputs a signal whose duty cycle is proportionate to the phase difference between its two inputs. This output is passed to the loop filter which is a low pass filter. This filter circuit outputs a DC voltage which is proportional to the duty cycle of the phase detector output, or in other words, the phase difference between the reference signal and the VCO output signal. The DC voltage thus obtained is used to



Phase locked loop diagram showing voltages

control the frequency of the output signal from the VCO.

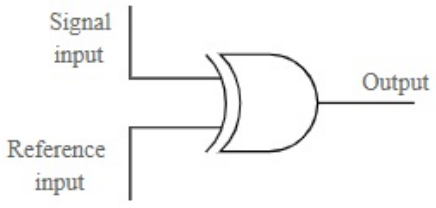
There is a feedback action involved. The VCO produces a signal which enters the phase detector. Here the phase of the signals from the VCO and the incoming reference signal are compared and a resulting difference in the form of an error voltage is produced. This error voltage is prpportional to the phase difference between the two signals. The error signal from the phase detector passes through a low pass filter which removes any high frequency elements on the signal and outputs a near DC signal. This error signal is applied to the control terminal of the VCO as its tuning voltage. This voltage is has polarity such that it tries to reduce the phase difference and hence the frequency difference between the two signals. Initially the loop will be out of lock, and the error voltage will pull the frequency of the VCO towards that of the reference, until it cannot reduce the error any further and the loop is locked.

When the phase locked loop is in a lock state, a steady state error voltage is produced. By using an amplifier between the phase detector and the VCO, the actual error between the signals can be reduced to very small levels. However some voltage must always be present at the control terminal of the VCO as this is what puts onto the correct frequency.

The fact that a steady error voltage is present means that the phase difference between the reference signal and the VCO is not changing. As the phase between these two signals is not changing means that the two signals are on exactly the same frequency.

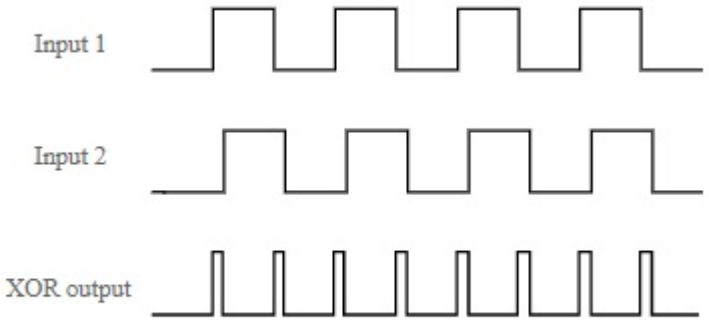
The phase locked loop, PLL is a very useful building block, particularly for radio frequency applications. The PLL forms the basis of a number of systems including the indirect frequency synthesizer, a form of FM demodulator and it enables the recovery of a stable continuous carrier from a pulse waveform. In this way, the phase locked loop, PLL is an essential similar waveRF building tool.

Phase sensitive detector: There are several possible ways for obtaining phase difference between two identical sine waves. A convenient way is to use an XOR gate which is a digital logic gate. So first of all, the sinusoidal waveform is converted into a square wave (compatible with the digital logic). The XOR gate based comparator has two inputs. The XOR gate outputs logic 0 signal when the two inputs are at same level, either low or high. And it outputs logic 1 signal when the one input is high and the other is low.



Exclusive OR phase detector

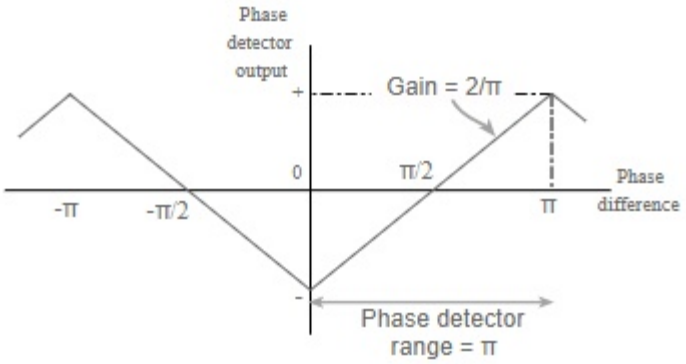
The way in which an exclusive OR, XOR phase detector works can be seen in the diagram below:



XOR phase detector response waveforms

Whenever the two inputs are at different levels the output is high. This generates a pulse train in which the pulse widths are proportional to the phase difference between these two signals.

It is important that the duty cycle of the inputs provided to the phase detector be 50%.. Otherwise it will lock in with a phase error. One more point worth noting is that the XOR based phase comparator is independent of input amplitude and constant over a π phase range.



XOR phase detector response curve

The characteristic of the phase detector is as shown in the adjacent figure. One can see that within the range of ±π, the phase detector output is a linear function of phase difference.

Voltage Controlled Oscillator

A Voltage controlled oscillator is a circuit that outputs a sine wave whose frequency can be controlled within a particular range by applying a DC voltage at its control input terminal. The design of a VCO is module can be quite complex. It requires sound theoretical design, followed by careful choice of all the components and then a good PCB layout. Even with circuit simulator, it may take a couple of iterations to design a good VCO. There are several parameters that must be considered during the design process. Some of these parameters are folowing:

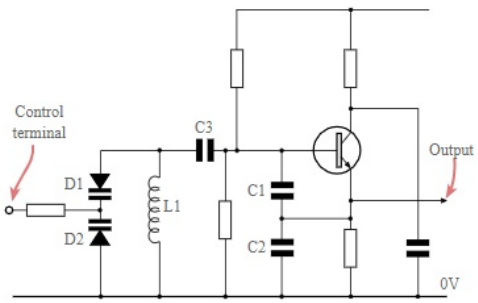
- ***VCO tuning range:*** It is obvious that the voltage controlled oscillator must be able to tune over the range that the loop is expected to operate over. This requirement is not always easy to meet and may require the VCO or resonant circuit to be switched in some extreme circumstances.
- ***VCO tuning gain:*** The gain of the voltage controlled oscillator is important. It is measured in terms of volts per Hz (or V/MHz, etc). As implied by the units it is the tuning shift for a given change in voltage. The voltage controlled oscillator gain affects some of the overall loop

design considerations and calculations. The VCO response curves can be seen to be relatively straight at lower frequencies. However they normally flatten out at higher voltages where the changes in capacitance reduce.

- ***VCO V/f slope:*** It is a key requirement for any voltage controlled oscillator used in a phase locked loop that the voltage to frequency curve is monotonic, i.e. it always changes in the same sense, typically increasing frequency for increasing voltage. If it changes, as can happen in some instances normally as a result of spurious resonances, etc, this can cause the loop to become unstable. Accordingly, this must be prevented if the phase locked loop is to operate satisfactorily.
- ***Phase noise performance:*** The phase noise performance of the voltage controlled oscillator is of particular importance in some PLL applications – particularly where they are used in frequency synthesizers. The phase noise performance of the voltage controlled oscillator is the dominant factor of phase noise outside the PLL loop bandwidth. Although close in noise is reduced by the action of the PLL, outside the loop bandwidth there is no reduction of VCO phase noise.

Oscillator circuit: A VCO can be constructed using an amplifier and a feedback loop. The gain of the amplifier is denoted as A and the feedback factor as B. For the circuit to oscillate the total phase shift around the loop must be 360° and the gain must be unity. In this way signals are fed back round the loop so that they are additive and as a result, any small disturbance in the loop is fed back and builds up. In view of the fact that the feedback network is frequency dependent, the build-up of signal will occur on one frequency, the resonant frequency of the feedback network, and a single frequency signal is produced. Many oscillators and hence VCOs use a common emitter circuit. This in itself produces a phase shift of 180°, leaving the feedback network to provide a further 180°.

For the oscillator to oscillate at a given frequency, the system includes a resonant circuit to ensure that the oscillation occurs on a given frequency. The resonant circuit can be one of a number of configurations from an LC resonant circuit in either series or parallel resonance dependent upon the circuit, or a quartz crystal, etc.



Voltage controlled oscillator circuit

A colpitts oscillator is often used for this purpose. The Colpitt's oscillator consists of an active device such as a bipolar transistor with capacitors placed between the base and emitter (C1) and the emitter and ground (C2) fulfils the criteria required for providing sufficient feedback in the correct phase to produce an oscillator. For oscillation to take place the ratio C1 : C2 must be greater than one.

The resonant circuit is made by including a inductive element between the base and ground. In the Colpitts circuit this consists of just an inductor, whereas in the Clapp circuit an inductor and capacitor in series are used.

The conditions for resonance is that:

$$f^2=\frac{1}{4\pi LC}$$

The capacitance for the overall resonant circuit is formed by the series combination of the two capacitors C1 and C2.

Thus the series capacitance is:

$$\frac{1}{C_t}=\frac{1}{C_1}+\frac{1}{C_2}$$
$$C_t=\frac{C_1C_2}{C_1+C_2}$$

In order to tune the oscillator for different frequencies, it is necessary to vary the resonant point of the circuit. This is best achieved by adding a capacitor across the inductor in the case of the Colpitts oscillator.

VCO tuning

To make a VCO, the oscillator needs to be tuned by applying a voltage. This can be achieved by making a variable capacitor using varactor diodes. The tuning voltage for the VCO can then be applied to the varactors.

Note that the control line from the phase detector is isolated from the varactor diodes using a resistor. RF chokes do not work well as they become part of the resonant circuit and tend to introduce the possibility of spurious resonances and non-monotonic V/f curves. Resistor values around 10kΩ often work well. With a value much lower than 10kΩ, an insufficient RF isolation is provided and this can lower the Q of the tuned circuit; On the other hand, for a value much higher than this, the source impedance may become too high. A little experimentation may be needed to find the optimum value.

The series capacitor C3 is used to block the DC from the inductor otherwise it would provide a direct short to ground and upset the bias arrangements of the circuit. Its value is normally large in comparison with C1 and C2 and can be ignored from the resonance perspective.

Loop Filter:

The Loop Filter is simply a Low pass filter. Its purpose is to integrate the PSD output so as to obtain a DC voltage proportional to its duty cycle. Recall that the duty cycle of the PSD output is

proportionate to the fraction of the signal cycle in which the displacements of the two waves have opposite polarity. This fraction is maximum when phase difference is $\pm\pi/2$ and minimum when the ecause tphase difference is 0. So when this is integrated, it gives a DC signal which can vary between maximum value when the phase difference is $\pi/2$ and zero when the phase difference is 0.

Since a Loop filter is simply a low pass filter, its actual circuit as shown in the figure, can be quite simple. But the circuit needs careful designing since several aspects of its operation critically depend on its design.

The range of Loop filter output voltages between the two limits of phase difference obtained from the PSD, i.e. $\pi/2$ and zero corresponds to the range of frequencies which the PLL can lock in to. The following points need to be considered in choosing a Loop filter circuit:

1. ***Filter comparison frequency:*** One of the major functions of the loop filter is to remove unwanted components of the phase detection or phase comparison frequencies. If they appear at the input to the VCO, then sidebands will appear offset from the carrier by a frequency equal to the phase comparison frequency.
2. ***Loop stability:*** The break points and roll off of the loop filter are of particular importance. The filter should be designed to give the required fall in loop gain at the unity gain point for the loop, otherwise the loop can become unstable.
3. ***Transient response / tracking:*** In some applications it may be necessary for the phase locked loop to track another signal or change frequency. The loop filter acts to slow the response down. The narrower the loop bandwidth, i.e. the lower the cut-off frequency of the filter, the slower the response of the loop to responding to changes. Conversely if the loop requires a fast response to changes in frequency, then it will need a wide loop bandwidth.

PLL modes of operation: The PLL works in two modes. When the conditions are suitable, then the VCO output frequency matches with the input signal frequency. This is the Lock mode. Otherwise the VCO gives an output at a characteristic frequency. This mode is called the free running mode. When the circuit is switched ON, the VCO is operating in free running mode. At this time, the input signal and the VCO output are at different frequencies. The PSD output has a non-zero value. When given to the VCO it impells the VCO to increase or decrease its frequency to make it match with the current input signal. If the input signal frequency changes, the PLL tracks this change and produces a VCO output that matches with the input signal frequency. The DC voltage output of the Loop filter gives the phase difference between the two signals.

Mathematical treatment (optional):

Linear PLL analysis:

If the input signal to the PLL is a sine wave:

$$r(t)=A\sin(\omega_r t+\theta_r)$$

and the output signal for the VCO is assumed to be

$$y(t)=A\cos(\omega_y t+\theta_y)$$

The phase detector is a multiplier so the output from the phase detector is just the product of the reference and VCO signals

$$e(t)=KA\sin(\omega_r t+\theta_r)\cos(\omega_y t+\theta_y)$$

This can be expanded to give $e(t)=\frac{KA}{2}\left[\sin((\omega_r+\omega_y)t+\theta_r+\theta_y)+\sin((\omega_r-\omega_y)t+\theta_r-\theta_y)\right]$

The first term on the right of the above expression is a high frequency term that is filtered out by the low pass loop filter. If we also assume that $\omega_r\approx\omega_y$ then the output from the multiplier can be approximated by:

$$e(t)=K_m[\theta_r-\theta_y]$$

The error signal is a gain multiplied by the phase difference between the reference signal and the signal from the VCO. Typically the LPF is a first order low pass filter

$$F(s)=\frac{K_f}{\tau_f s+1}$$

and since phase is the integral of angular velocity the VCO is modelled as $VCO(s)=\frac{K_0}{s}$

Combining these transfer functions gives the loop gain

$L(s)=\frac{K_1}{s(\tau_f s+1)}$ where $K_1=K_m K_f K_0$

which will be recognised as the transfer function of a position servo [2]. So the closed-loop dynamics are $T(s)=\frac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}$ where $\omega_n=\sqrt{\frac{K_1}{\tau}}$ and $\zeta=\frac{1}{2\sqrt{\tau K_1}}$

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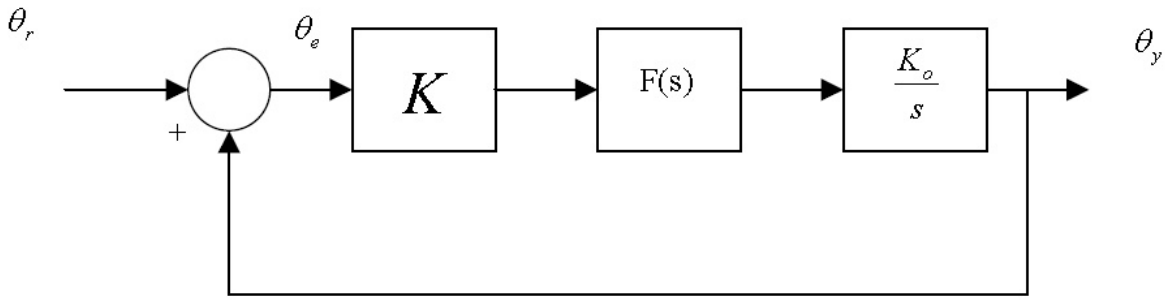
This is a standard second order transfer function with natural frequency ω_n and damping ζ. The block diagram of the linear approximation to the PLL is shown in Figure below. Here θ_r and θ_y are the reference signal and VCO phase shift respectively.



Linear approximation of a Phase Locked Loop

Applications:

Following are some of the common applications of PLL. (1) Frequency synthesizers that provide multiples of a reference signal frequency, (2) FM demodulation networks for FM operation with excellent linearity between the input signal frequency and the PLL output voltage, (3) Demodulation of the two data transmission or carrier frequencies in digital-data transmission used in frequency-shift keying (FSK) operation. Apart from these there is a wide variety of areas where a PLL is used, including in modems, telemetry receivers and transmitters, tone decoders, AM detectors, and tracking filters. The phase locked loop is found in many wireless, radio, and general electronic items from mobile phones to broadcast radios, televisions to Wi-Fi routers, walkie talkie radios to professional communications systems and vey much more.

References:

1. PLL Phase Locked Loop Tutorial & Primer: :
https://www.electronics-notes.com/articles/radio/pll-phase-locked-loop/tutorial-primer-basics.php
2. Mark Christopher Readman (Stockprt College/Trafford College Group) (2003) Phase Locked Loops. Technical Report. DOI: 10.13140/RG.2.1.1076.2407